Introduction to Programmable Logic Devices


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Outline
- What is PLD
- Advantages of PLDs
- PLD Applications
- PLD Design Flow
- PLD Architecture
- The CPLD
- Using PLDs to Solve Basic Logic Designs
- Tutorial for Using Aletra’s Quartus II Design and Simulation Software
- FPGA Applications
What is PLD?

- A PLD is an electronic component used to build reconfigurable digital circuits. Before the PLD can be used in a circuit, it must be programmed.
- Any digital logic design can be implemented using PLDs.
- Four Types of PLDs:
  - SPLDs (Simple PLD)
  - CPLDs (Complex PLD)
  - FPGAs (Field Programmable Gate Array)
  - ASICs (Application Specific IC)

Fix Logic vs. Programmable Logic [3][4]

- The PLD Advantages:
  - Increase Integration: (Reduce the package count, increased features)
  - Lower power: (CMOS and fewer packages)
  - Lower cost:
    - Customer Off-the-self availability (short lead times for prototypes or production parts)
    - Does not require customers to pay for large NRE (Non-Recurring Engineering) costs
    - Available in any quantity and any time (reduce inventory cost)
  - Easier to Change:
    - More flexibility during the design cycle
    - Can be programmed, upgraded via the Internet
Implementing the Boolean Equation Using 7400 Series Logic ICs

- Figure 4-3 Implementing the Boolean equation $X = A'B + (B+C)'$ using 7400-series logic ICs: (a) Logic Diagram; (b) connection to chips

Implementing the Boolean Equation Using a PLD

- Figure 4-4 Implementing the Boolean equation $X = A'B + (B+C)'$ using a PLD
Figure 4-5 The Altera DE2 Development and Education Board

PLD Applications

- Glue Logic, required to design a microcomputer system
- State Machines
- Synchronization
- Decoders
- Counters
- Bus Interfaces
- Parallel-to-Serial
- Serial-to-Parallel
- Subsystems
- etc
**PLD Design Process/Flow**

1. Design Idea
2. Develop the equations to solve the required logic operations
3. Design Entering: Schematic Editor/VHDL Text Editor
4. Simulate the input/output conditions via timing waveform analysis
5. Compile the program
6. Program the PLD Chips
7. Test the final programmed PLD Chips via actual input/output signals

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**SPLD (Simple Programmable Logic Devices)**

- Manufacturers
  - Cypress, [http://www.cypress.com/?id=7&source=header](http://www.cypress.com/?id=7&source=header)
SPLD (Simple Programmable Logic Devices)

Figure 4-6 One-line convention for PLDs

W = AB
X = A\overline{B}
Y = \overline{A}B
Z = \overline{A}B

SPLD (Simple Programmable Logic Devices)

- Figure 4-7 PAL Architecture of an SPLD (programmable AND, fixed OR)

X = AB + A\overline{B} + \overline{A}B + \overline{A}B
SPLD (Simple Programmable Logic Devices)

- PAL (Programmable Array Logic)
  - A programmable logic device in which each output is computed as a two-level “Sum of Products” (an OR of ANDs) expression
  - Use a programmable “macro cell” on each output
  - Programmable AND, Fixed OR
  - Programming the PAL: blows the fuses
  - PAL16L8 (Figure 4-9) – an Example
    - 16 inputs, 8 outputs PAL16L8

- Programmable Logic Arrays (PLAs), [7]
  - Pre-fabricated building block of many AND/OR gates (actually implemented NOR/NAND)
  - Programmable array block diagram for implementing SOP form of logic equations
  - Programmable AND, Programmable OR

SPLD (Simple Programmable Logic Devices)

- Figure 4-8 PLA Architecture of an SPLD (programmable AND, programmable OR)
The CPLD

- Combining several PAL type SPLD into a single IC package
- Example: Altera MAX 7000S
- Consists of thousands of individual logic gates
- Nonvolatile (remember logic and interconnections through EEPROM)
- Figure 4-10 – Internal structure of a CPLD
Figure 4-10 Internal structure of a CPLD

Figure 4-11 $X = ABCD + AB'CD' + A'B'C'D'$: (a) implemented using 7400-series ICs; (b) implemented within a LUT of an FPGA (showing the flow for $ABCD$).
Figure 4-11  \( X = ABCD + AB'CD' + A'B'C'D' \): (a) implemented using 7400-series ICs; (b) implemented within a LUT of an FPGA (showing the flow for \( ABCD \)).

**Using PLD to Solve Basic Logic Design**

- Figure 4-12 FPGA Design Flows
Using PLD to Solve Basic Logic Design

- Figure 4-13
  (a) Block editor file
  (b) VHDL text editor
  (c) Simulation waveform file

Example 4-1

Example 4-1

Figure 4-14 shows five computer screens generated by the Quartus® II software. Each screen produces, or is the result of, a different logic circuit. Determine the Boolean equation that is being implemented in each case.

Solutions:
(a) \( X = A + B \)
(b) \( X = \overline{AB}C \)
(c) \( X = AB \)
(d) \( X = AB + \overline{BC} \)
(e) \( X = A + (BC) \)
\( Y = AB + \overline{B} + C \)
Example 4-1 Continue

(b) $X = (ABC)'$

(c) $Y = AB + (B+C)'$

Example 4-1 Continue

(b) $X = AB + B'C$

(c) $X = A + (BC')$